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OPERATIONAL TRANS-CONDUCTANCE AMPLIFIER WITH IMPROVED CHARACTARISTICS FOR ACTIVE FILTERS

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Abstract

Active clear out plays an critical function in today's global of communication. A famous application uses an op-amp to build lively filter out circuits. A filter out circuit may be constructed the usage of passive components: resistors and capacitors, Low pass and excessive skip filter out structure have sizeable utility and the usage of CMOS Operational Trans-conductance amplifier gives capability to perform properly in Nano-meter variety as it has better manage over short channel impact and different scaling problem like gate leakage, sub-threshold conduction. The proposed clear out includes OTA. This filter out suggests low sensitivity to passive components, low element count and simplicity in design.

Design of operational trans-conductance amplifier (OTA) is the principle awareness for designing excessive skip and low pass filter out. The simplicity and linearity are the important capabilities of the OTA intended for any application. There are several in contrast to OTA's are used wherein this OTA is a easy OTA with low energy intake in (µwatt) and high gain (db). The OTA is considered by numerous constraints like open loop gain, Bandwidth, Slew Rate, CMRR and etc. The output of OTA with HLF completed in mentor photographs 0.25µm technology [2].

Keywords: basic current mirror, differential amplifier, common source amplifier, active low pass, slew rate, high pass filter, gain, CMRR.

I: INTRODUCTION

Analogue filters play a very giant position in electronic system. Low pass filter out passes signal with a frequency lower than a certain cut-off frequency and attenuates sign with frequencies higher than the cut-off frequency. The designing of filter using passive ladder filter out as a prototype for lively filters, together with operational trans-conductance amplifiers and capacitors (OTA-C), has emerge as very popular. The designing of OTA is done on Mentor graphics EDA software. It is suite of gear for the design of included circuits. There are particularly 3 tools S-edit, W-edit, and L-edit.

Design of the op amp, accompanied by means of High Pass, Low Pass filters are first carried out on Schematic to test its Simulation by means of software of SPICE device to generate waveforms. Another tool of Tanner EDA is L-Edit and it's miles an incorporated circuit Physical design device it lets in us to draw layout of a circuit and take a look at cross-section, carry out DRC (Design Rule Check) and generate a Netlist of your Layout so that we can perform LVS (Layout Versus Schematic) using a calibrate tool.[3]

II. Literature Survey

Today Power Consumption has become associate degree more and more vital issue in filter. Antecedently filters were designed exploitation Bipolar semiconductor device amplifiers that are a circuit that deliver low-gain, high power consumption and additional noise amplification of the input [3] [4]. Op – amp give a really effective mean of making low pass and high pass filter while not the requirement for electrical device. Low pass and high pass filter exploitation op-amp may be utilized in many areas power provides to the output of digital to analogue converters to get rid of alias signals and plenty of additional application. However because the advancement takes place in technological world Operational Trans-conductance electronic equipment attains some deserves over bipolar devices [5].

A bipolar device is "current Controlled Amplifier" and has just one input whereas op-amp has two inputs.

III. Design and computer simulations

Design of operational trans-conductance electronic equipment (OP-AMP) [1] with active filters is that the main focus of this paper for planning high pass and low pass filter. The simplicity and one-dimensionality are the essential options of the OP-AMP supposed for any application. The Schematic of OP-AMP is shown in Figure one. The Op-amp is taken into account by numerous constraints like open gain, Bandwidth, Slew Rate, Noise and etc. [4]. The performance Measures are mounted Due to Design parameters love Transistors size (W/L), Bias current and etc. during this paper we tend to describe style of OP-AMP; this design is finished in Mentor graphic zero.25µm technology.The higher order filter will be designed to boost the frequency response and increase the sharpness of filter. They can be designed using different topologies like-cascade and passive ladder. The different types of filters like band pass, high pass and band reject filter can be realized using OTA and capacitor

III A. SCHEMATIC IMPLEMENTATION

The basic building blocks of Operational Trans-Conductance Amplifier are 1. Basic current mirror. 2. Differential amplifier 3. Common source amplifier.4.Low pass filter 5. High pass filter.

1. Current mirror is established to maintain current stability in whole circuit, it has MN1as source and MN2 as a mirror transistor and ammeter as a test point to measure mirror current, and which consumes less power because of its architecture nature.

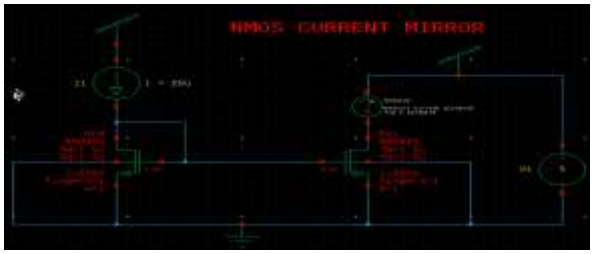

Fig: 1 current mirrors with 20µAms.

2. Differential amplifier

Basic building blocks of DS amplifier has MN3 as a Vin1,MN4 as aVin2, and Two MP1,MP2 are provided proper biasing for DS, Which amplifies the difference of the input stages.

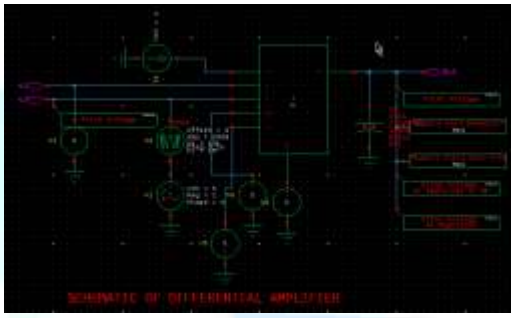

Fig: 2 Differential Amplifiers.

The below figures shows the simulation results of DS producing gain of 23.76dB with output voltage of15.35 volts

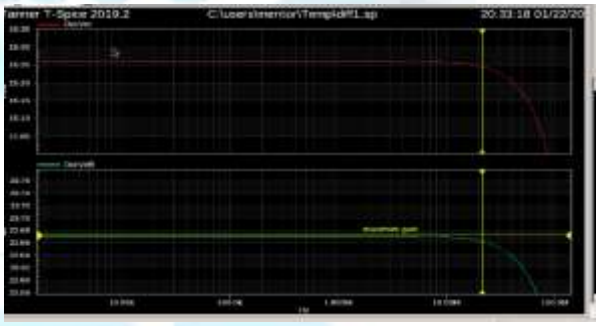

Fig: 3 Differential amplifier gains with phase.

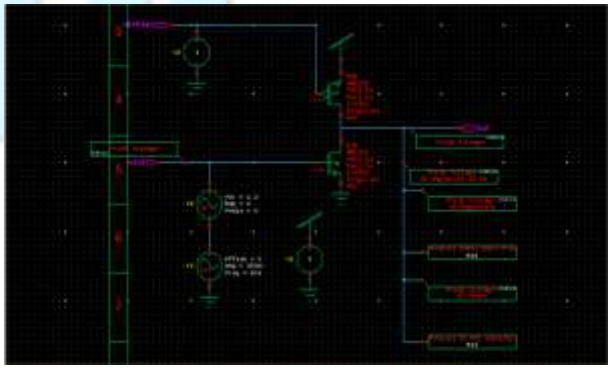

Fig: 4 common source amplifiers.

From the Schematic we can observe that two transistors are used i.e one PMOS and one NMOS transistor.

Two supply voltages are used one is 3v and other is 5v respectively. A sinusoidal AC signal is given with an offset of 0v

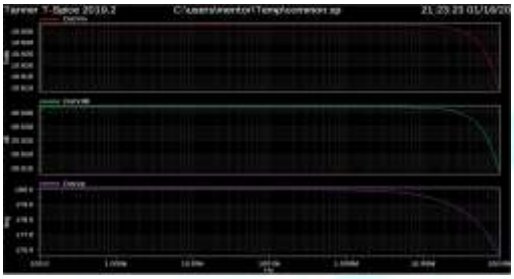

Fig: 5. Gain plot of common source amplifiers

From the output we can observe that the gain of Common Source amplifier is **20.63dB.**where V_{out} is **10.63v** and V_{in} is **0.53v.**

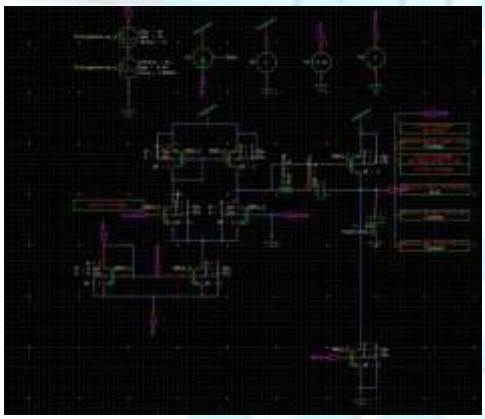

Fig6. OPERATIONAL AMPLIFIER

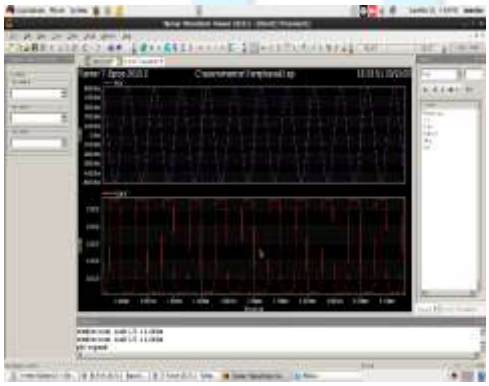

Fig 7: output and input response of op-amp

The above figure 7 shows the simulation results of op amp with input voltage of 500 millivolts produces 2.5 volts as aoutput.

Fig 8: gain with phase plot of op amp

The above figure 8 shows the gain simulation results of operational amplifier with 35 db, with input voltage of 500 millivolts.

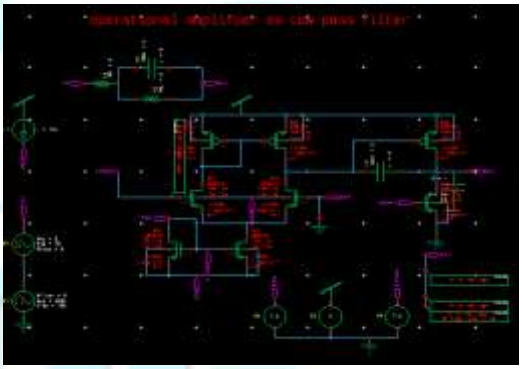

Fig 9: OP AMP with LPF schematic

The above figure9 shows Low pass filter schematic with100nf capacitance R1= 100 Kohms.

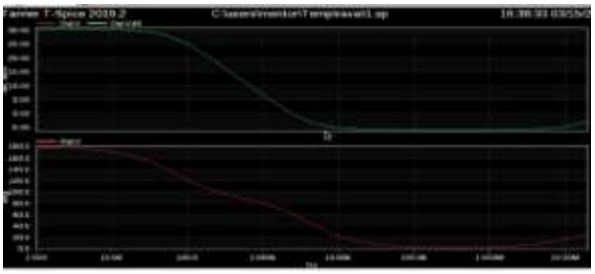

Fig10.LPF with gain plot

The above figure 10 shows low pass filter with lower cutoff frequency of 100 Hz.

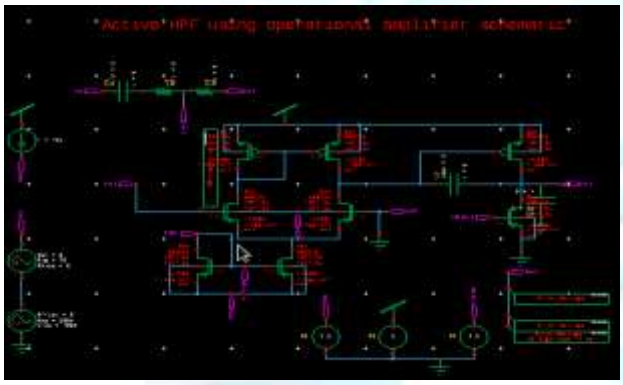

Fig 11. Op amp with HPF

The above shows schematic of HPF with feedback resistance of R15K, R1=1.5K ohms with input capacitance of 4.7nf.

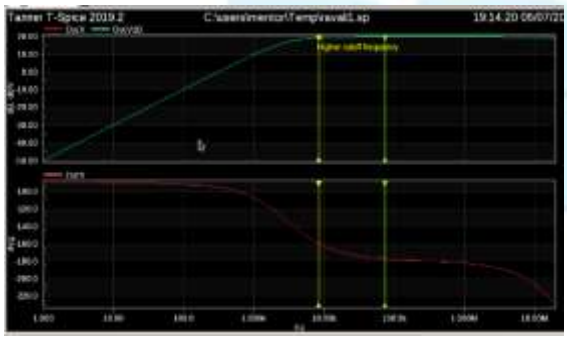

Fig 12: gain of HPF

The above figure shows simulation of gain plot with higher cutoff frequency of 10 KHz.

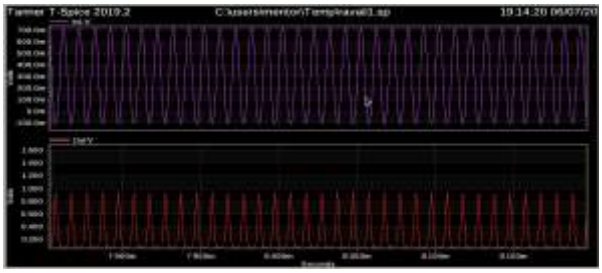

Fig 13:Output OF HPF.

The above figure shows output of HPF with V_{in} 700millivolts which produce V_{out} as 2.60Volts.

IV Design rules, layouts and Result

As the length between the source and drain is 250nm or channel length, [5] we are using 250nm Technology [6].

PMOS			
S.NO	FIELD COMPONENTS	LENGTH	WIDTH
1.	N-WELL	2.995	4.110
2.	SUBSTRATE	1.050	1.050
3.	P IMPLANT	2.005	2.065
4.	GATE	2.100	0.250
5.	METAL	1.140	0.545
6.	GROUND	4.170	0.645

Table 1: PMOS design rules.

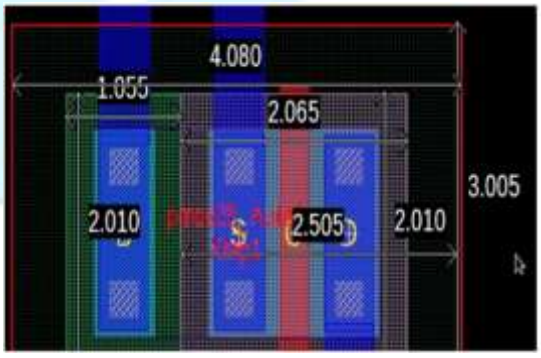

Fig: 14 Design rules for PMOS.

NMOS			
S.NO	FIELD COMPONENTS	LENGTH	WIDTH
1.	P-WELL	2.045	2.000
2.	SUBSTRATE	1.990	1.010
3.	N IMPLANT	1.550	1.495
4.	GATE	2.095	0.250
5.	METAL	3.710	0.625

Table 2: Design rules for NMOS.

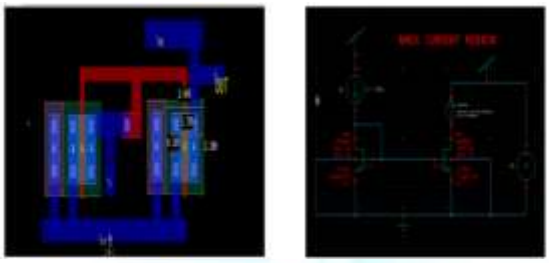

Fig: 15 layout of current mirror

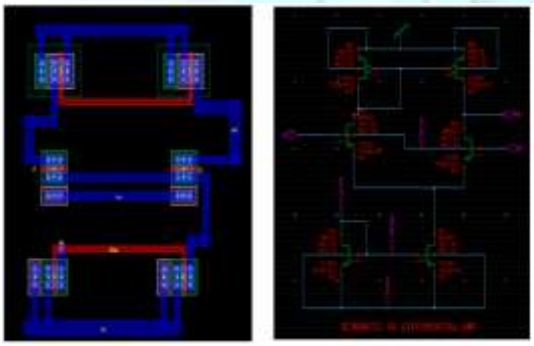

Fig16: Design rules for Differential amplifier.

Fig 17: DRC report by calibrate tool

IV Calculations

1. Trans conductance Amplifier (gm):

The ratio of the change in current at the output terminal to the change in the voltage at the inputterminal of an active device.

$$gm = Ids/ Vgs$$

Where Vgs = 500milli, Ids = 1.5 milli
Gm= 0.003

2. SLEWRATE:

How fast vout can follow the input signal
SR= change in Vout to change in time interval

$SR = 2.2/ 0.2 \times 10^{-3}$
SR = 0.012 V/µs.

3. CMRR(COMMON MODE REJECTION RATIO):

CMRR has the ability of an op amp to reject any signal common to both inputs of the op amp

$$CMRR = R_1+R_F/R_1 \text{ X } Vin/Vout.$$

For LPF:
Where R_1=10 KΩ, R_f=100 KΩ, Vin = 0.5volts, gain = 30db.
CMRR (LPF) = 1.964.
CMRR in db = 5db.

For HPF:
Where R_1=1.5KΩ, R_f=15KΩ, Vin = 0.7volts, Vout = 2.60, gain = 20db.
CMRR (LPF) = 3.9.
CMRR in db = 11.8 db.

V Conclusion and to be Research

In this project we haveshown that how a low pass and high pass filter designed using operational trans-conductance amplifier can reduce the power consumption in the circuit. A filter circuit can be constructed using passive components: resistors and capacitors , Low pass and high pass filter structure have widespread application and using CMOS Operational Trans-conductance amplifier gives capability to perform well in Nano- meter range as it has better control over short channel effect and other scaling

problem like gate leakage, sub-threshold conduction. The proposed filter consists of OTA .The other advantages of our design less power consumption, CMRR & Slew rate are better, gain is high. By this schematic we are proposing to design second order low pass and high pass filter devices and then go for power optimization.

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